In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 8, line 29 to page 9, line 13 as follows:

--The set portion ~~510~~ 520 (bits 13-5) indicates to which set the address maps. In case of direct-mapped caches as in this example, a set is equivalent to a line frame 425. For the address 0020h, the set portion is 1. Cache controller 410 includes tag comparator 412 which compares the tag portion ~~520~~ 510 (bits 14 to 31) of address 400 with the tag from tag RAM 422 of the indicated set. Cache controller 410 ANDs the state of the corresponding valid bit 421 with the tag compare result in AND gate 413. A 0 result is a miss, the cache does not contain the instruction address sought. This could occur if the address tag portions do not match or if the valid bit 421 is 0. A 1 result is a hit, the cache stores the instruction address sought. Since we assumed that all valid bits 421 are 0, cache controller 410 registers a miss, that is the requested address is not contained in cache.--